WHAT IS CLAIMED IS:

1. A decoding system for producing pieces of video data information representative of plural kinds of pictures to be reproduced on a screen of a display from compressed data streams having bit strings representative of said plural kinds of pictures and coded through an inter-frame predictive coding technique, comprising:

plural memories respectively assigned to said compressed data streams, each of said plural memories having plural frame memories more than frame memories required for producing any one of said pieces of video data information;

a decoding section selectively supplied with said bit strings of said compressed data streams, and producing output signals representative of said pieces of video data information and a first control signal representative of one of said plural kinds of picture represented by the bit string just processed;

an information processor connected to said decoding section, producing the pieces of video data information from said output signals or through an information processing between the pieces of video data information represented by said output signals and the pieces of video data information already stored in said plural memories, and storing each of said pieces of video data information in one of said plural frame memories of the associated one of said plural memories; and

a controller responsive to said first control signal so as to select one of said plural frame memories of associated one of said plural memories, and in-

structing said information processor to transfer the piece of video data information produced from said bit string just processed to said one of said plural frame memories for replacing an invalid piece of video data information already stored therein with said piece of video data information.

2. The decoding system as set forth in claim 1, in which said compressed data streams are coded on the basis of standards of motion picture experts group, and said plural kinds of pictures are an I-picture coded in a frame without any piece of video data information in a different frame, a P-picture coded in a frame with reference to a piece of video data information in a first predetermined frame before said frame and a B-picture coded in a frame with reference to a piece of video data information in a second predetermined frame before said frame and a third predetermined frame after said frame.

3. The decoding system as set forth in claim 2, in which said B-picture requires three frame memories for producing said piece of video data information to be stored, and each of said plural memories contains four frame memories.

4. The decoding system as set forth in claim 2, in which plural pictures selectively categorized in said I-picture, said P-picture and said B-picture are concurrently reproduced on said screen in a single frame period, and said I-picture and said P-picture serve as a core picture.

5. The decoding system as set forth in claim 4, further comprising a synchronous signal generator producing a first synchronous signal supplied to

said controller and a second synchronous signal supplied to said display for reading out said piece of video data information.

6. The decoding system as set forth in claim 5, in which said controller includes

a timing generator responsive to said first synchronous signal so as to generate plural initiation signals in each frame period at intervals,

plural frame memory controllers respectively associated with said compressed data streams and each responsive to said first control signal so as to selectively produce a second control signal representative of one of said plural frame memories of the associated memory for writing the piece of video data information thereinto, a third control signal representative of another of said plural frame memories of said associated memory for reading out the piece of video data information therefrom and a fourth control signal representative of yet another of said plural frame memories of said associated memory for reading out the piece of video data information, and

an address generator responsive to said second, third and fourth control signals so as to produce address signals selectively supplied to said plural memories.

7. The decoding system as set forth in claim 6, in which each of said plural frame memory controllers includes

a set of programmed instructions stored in an information storage medium, and

a data processor connected to said information storage medium and sequentially executing said programmed instructions so as to realize

a first means for defining a first variable indicative of one of said plural frame memories for storing the latest core picture, a second variable indicative of another of said plural frame memories for storing another core picture prior to said latest core picture, a third variable indicative of yet another of said plural frame memories for storing the latest B-picture, a fourth variable indicative of still another of said plural frame memories presently unused and a fifth variable used as a temporary storage,

a second means transferring the contents of said third, fourth and fifth variables to said fifth, third and fourth variables, respectively, for changing the contents of said fifth, third and fourth variables when said bit string presently processed is representative of said B-picture,

a third means transferring the contents of said second, first, fourth and fifth variables to said fifth, second, first and fourth variables, respectively, for changing the contents of said fifth, second, first and fourth variables when said bit string presently processed is representative of said core picture, and

a fourth means producing said second control signal indicative of the contents of said third variable when said bit string presently processed is representative of said B-picture, said fourth means producing said second control signal indicative of the contents of said first variable when said bit string presently processed is representative of said core picture.

8. The decoding system as set forth in claim 6, in which each of said plural frame memory controllers includes

a first flip-flop circuit having a first input node, a first output node for producing said fourth control signal and a first control node supplied with a first enable signal,

a second flip-flop circuit having a second input node connected to said first output node, a second output node for producing said third control signal and a second control node supplied with said first enable signal,

a third flip-flop circuit having a third input node, a third output node and a third control node supplied with a second enable signal,

a fourth flip-flop circuit having a fourth input node, a fourth output node connected to said first input node and said third input node and a fourth control node supplied with a third enable signal,

a first selector having a fifth input node connected to said second output node, a sixth input node connected to said third output node and a fifth output node connected to said fourth input node and responsive to a selecting signal for selectively connecting said fifth input node and said sixth input node to said fifth output node,

a second selector having a seventh input node connected to said first output node, an eighth input node connected to said third output node and a sixth output node for outputting said second control signal and responsive to said first selecting signal for selectively connecting said seventh input node and said eighth input node to said sixth output node, and

a signal generator responsive to associated one of said plural initiation signals and said first control signal so as to produce said first enable signal, said second enable signal, said third enable signal and said selecting signal,

said first enable signal being changed to an active level when said one of said plural initiation signals and said first control signal are indicative of an active and said core picture, respectively,

said second enable signal being changed to said active level when said one of said plural initiation signals and said first control signal are indicative of said active level and said B-picture, respectively,

said third enable signal being changed to said active level when said one of said plural initiation signals and said first control signal are indicative of said active level and one of said core picture and said B-picture, respectively,

said selecting signal causing said first selector and said second selector to connect said fifth input node and said seventh input node to said fifth output node and said sixth output node when said first control signal is indicative of said core picture,

said selecting signal causing said first selector and said second selector to connect said sixth input node and said eighth input node to said fifth output node and said sixth output node when said first control signal is indicative of said B-picture.

9. The decoding system as set forth in claim 1, further comprising a selector having plural input nodes respectively supplied with said compressed data

streams and an output node connected to said decoding section and transferring the bit strings from said plural input nodes to said output node in a time sharing fashion.

10. The decoding system as set forth in claim 9, in which said decoding section includes

a variable length decoder connected to said output node of said selector and producing decoded signals from said bit strings,

an inverse quantizer connected to said variable length decoder and producing quantized signals from said decoded signals, and

a two-dimensional inverse discrete cosine converter connected between said inverse quantizer and said information processor and producing converted signals from said quantized signals.

11. A method for concurrently reproducing plural pictures on a screen of a display, comprising the steps of:

a) selectively supplying plural bit strings respectively extracted from plural compressed data streams to a decoding section in a time sharing fashion for producing pieces of video data information representative of said plural pictures in a first frame period;

b) selecting unused frame memories from plural memories each consisting of plural frame memories more than frame memories required for producing one of said pieces of video data information representative of one of said plural pictures in said first frame period,

c) storing said pieces of video data information in said unused frame memories in said first frame period, and

d) transferring said pieces of video data information from said unused frame memories to a display in a second frame period after said first frame period while other pieces of video data information are being stored in other unused frame memories.

12. An information storage medium for storing a set of programmed instructions to be executed by a data processor, said set of programmed instructions realizing a method for concurrently reproducing plural pictures on a screen of a display, comprising the steps of:

a) selectively supplying plural bit strings respectively extracted from plural compressed data streams to a decoding section in a time sharing fashion for producing pieces of video data information representative of said plural pictures in a first frame period;

b) selecting unused frame memories from plural memories each consisting of plural frame memories more than frame memories required for producing one of said pieces of video data information representative of one of said plural pictures in said first frame period,

c) storing said pieces of video data information in said unused frame memories in said first frame period, and

d) transferring said pieces of video data information from said unused frame memories to a display in a second frame period after said first frame

period while other pieces of video data information are being stored in other unused frame memories.